UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,559	09/27/2001	Jian-Hsing Lee	0941-0332P-SP	8922

2292 7590 07/29/2003

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER
BENENSON, BORIS

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 07/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/963,559	Applicant(s) LEE ET AL.
	Examiner Boris Benenson	Art Unit 2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Specification

1. The abstract of the disclosure is objected to because a diode string on page 5 lines 3 and 5 referenced as 141, but on line 16 and on Figure 3 the same diode string is referenced as 441. Correction is required. See MPEP § 608.01(b).

Drawings

2. The drawings are objected to because on Figure 3 an arrow below a diode string should be a diode, connected in opposite direction. Gates of two PMOS and one NMOS in the driving circuit are " floating". Is it intentional or an error? A label "N1" should be related to a diode string (441) in the Voltage Detecting Device (44), not in the Driving Circuit (48). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at

> the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art in view of Ker et al. (5,959,820). Prior art disclosed in the application describe an electrostatic discharge protection device that is located between a pad and an internal circuit, and is coupled to a first level signal and a second level signal, comprising:

a. a signal converting device for outputting the second level signal when the detected result signal is received;

b. a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch has a first controlling gate and turns on when the voltage level of the pad reaches a second predetermined voltage level;

c. a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch has a second controlling gate and turns on and raises the voltage value of the first level signal when the voltage level of the pad reaches a third predetermined voltage level;

d. a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch has a third controlling gate and turns on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the second level signal.

The Prior Art doesn't disclose a device for detecting the voltage level of the first level signal, wherein when the voltage level of the first level signal reaches a first predetermined value, the voltage-detecting device outputs a detecting result signal. Ker et al. teach a voltage based ESD detection circuit (Fig. 11, Pos. 204). Ker et al. provide multiple ways for implementation of such ESD detection circuits including a diode string (Fig. 14 b, Pos. 204 d). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Prior Art with Ker et al. teachings and connect a voltage based ESD detection circuit to switching circuit (NOR logic element), because it will allow to detect increase of Vcc (internal) above a predetermine level and enable ESD protection.

Referring to Claims 2 and 12, the first and the third switch in Applicant Admitted Prior Art are NMOS transistors.

Referring to Claims 3 and 13, the second switch in Applicant Admitted Prior Art is PMOS transistor.

Referring to Claim 4, Ker et al. teach a voltage detection circuit comprising at least one serial diode and turn-on voltage of the serial diodes is between the first level signal (Vdd) and the first predetermine voltage level.

Referring to Claims 5-10 and 14-19, the Applicant Admitted Prior Art, modified by teachings of Ker et al. provides all the limitation of Claims 5-10 and 14-19.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (703) 305-6917. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Boris Benenson
Examiner
Art Unit 2836

B.B.
July 23, 2003

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER